WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device formed on a surface of a semiconductor substrate, comprising:

a memory transistor having a floating gate and a control gate successively formed above a first well region of said semiconductor substrate, having its threshold voltage set to a first voltage for storing a data signal at a first logic level, and having its threshold voltage set to a second voltage level for storing a data signal at a second logic level;

a reference transistor having a floating gate and a control gate successively formed above a second well region of said semiconductor substrate, and having its threshold voltage set to a reference voltage between said first and second voltages;

a read circuit reading the threshold voltages of said memory transistor and said reference transistor;

a comparison circuit comparing the threshold voltage of said memory transistor read by said read circuit with the threshold voltage of said reference transistor read by said read circuit and outputting a pulse waveform instruction signal based on a comparison result; and

a data signal rewriting circuit supplying a pulse signal train having a pulse waveform in accordance with said pulse waveform instruction signal between the control gate of said memory transistor and said first well region and changing the threshold voltage of said memory transistor from said first voltage to said second voltage.

2. The nonvolatile semiconductor memory device according to claim 1, comprising a plurality of reference transistors, threshold voltages of said plurality of reference transistors being set respectively to a plurality of reference voltages different from each other, wherein

said read circuit reads the threshold voltages of said memory transistor and said plurality of reference transistors, and

said comparison circuit compares the threshold voltage of said memory transistor read by said read circuit with each of the threshold

voltages of said plurality of reference transistors read by said read circuit and outputs said pulse waveform instruction signal based on a comparison result.

3. The nonvolatile semiconductor memory device according to claim 1, comprising a plurality of reference transistors, threshold voltages of said plurality of reference transistors being set together to said reference voltage, wherein

said read circuit reads the threshold voltage of said memory transistor and a mean value of the threshold voltages of said plurality of reference transistors, and

said comparison circuit compares the threshold voltage of said memory transistor read by said read circuit with the mean value of the threshold voltages of said plurality of reference transistors read by said read circuit and outputs said pulse waveform instruction signal based on a comparison result.

4. The nonvolatile semiconductor memory device according to claim 1, comprising:

a plurality of memory blocks each including a plurality of memory transistors;

a plurality of reference transistors provided respectively corresponding to said plurality of memory blocks; and

a decoder selecting any memory block of said plurality of memory blocks and any memory transistor of a plurality of memory transistors belonging to the memory block, and a reference transistor corresponding to the memory block, in accordance with an address signal, wherein

said read circuit reads the threshold voltages of the memory transistor and the reference transistor selected by said decoder, and

said data signal rewriting circuit changes the threshold voltage of the memory transistor selected by said decoder from said first voltage to said second voltage.

5. A nonvolatile semiconductor memory device formed on a surface of a semiconductor substrate, comprising:

a reference transistor and a memory transistor, each having a floating gate and a control gate successively formed above a well region of said semiconductor substrate, having its threshold voltage set to a first voltage for storing a data signal at a first logic value, and having its threshold voltage to a second voltage for storing a data signal at a second logic level;

a read circuit reading the threshold voltage of said reference transistor;

a comparison circuit comparing the threshold voltage of said reference transistor read by said read circuit with a reference voltage between said first and second voltages and outputting a pulse waveform instruction signal based on a comparison result; and

a data signal rewriting circuit supplying a pulse signal train having a pulse waveform in accordance with said pulse waveform instruction signal between the control gate of each of said reference transistor and said memory transistor and said well region and changing each of the threshold voltages of said reference transistor and said memory transistor from said first voltage to said second voltage.

6. The nonvolatile semiconductor memory device according to claim 5, wherein said comparison circuit compares the threshold voltage of said reference transistor read by said read circuit with each of a plurality of reference voltages different from each other between said first and second voltages and outputs said pulse waveform instruction signal based on a comparison result.

7. The nonvolatile semiconductor memory device according to claim 5, comprising a plurality of reference transistors, wherein

said read circuit reads a mean value of threshold voltages of said plurality of reference transistors, and

said comparison circuit compares said reference voltage with the

mean value of threshold voltages of said plurality of reference transistors and outputs said pulse waveform instruction signal based on a comparison result.

8. A nonvolatile semiconductor memory device formed on a surface of a semiconductor substrate, comprising:

a memory transistor having a floating gate and a control gate successively formed above a first well region of said semiconductor substrate, having its threshold voltage set to a first voltage for storing a data signal at a first logic level, and having its threshold voltage set to a second voltage lower than said first voltage for storing a data signal at a second logic level;

a first read circuit reading the threshold voltage of said memory transistor;

a voltage generation circuit generating a third voltage between said first and second voltages;

a comparison circuit comparing the threshold voltage of said memory transistor read by said first read circuit with said third voltage generated by said voltage generation circuit, outputting a first pulse waveform instruction signal, if the threshold voltage of said memory transistor is between said first and third voltages, and outputting a second pulse waveform instruction signal, if the threshold voltage of said memory transistor is between said third and second voltages; and

a data signal rewriting circuit supplying a pulse signal train between the control gate of said memory transistor and said first well region and decreasing the threshold voltage of said memory transistor from said first voltage to said second voltage, wherein

said data signal rewriting circuit keeps a pulse signal interval constant, continuously raises an amplitude voltage of said pulse signal train by a prescribed value per one pulse signal, sets each pulse signal width at a first width, if said first pulse waveform instruction signal is output from said comparison circuit, and sets each pulse signal width at a second width greater than said first width, if said second pulse waveform instruction signal is output from said comparison circuit.

9. The nonvolatile semiconductor memory device according to claim 8, wherein said voltage generation circuit includes

a reference transistor having a floating gate and a control gate successively formed above a second well region of said semiconductor substrate, and having its threshold voltage set to said third voltage, and

a second read circuit reading the threshold voltage of said reference transistor.

10. The nonvolatile semiconductor memory device according to claim 8, wherein

said voltage generation circuit further generates a fourth voltage between said third and second voltages,

said comparison circuit further compares the threshold voltage of said memory transistor read by said first read circuit with said fourth voltage generated by said voltage generation circuit and outputs a third pulse waveform instruction signal if the threshold voltage of said memory transistor is between said fourth and second voltages, and

said data signal rewriting circuit further sets each pulse signal width at a third width smaller than said second width if said third pulse waveform instruction signal is output from said comparison circuit.